REMARKS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe the subject matter which applicant regards as the invention.

The Examiner objected to the abstract indicating that the abstract should be within the range of 50-150 words. Applicant notes that the abstract has been amended to overcome the Examiner's objection.

The Examiner rejected claims 1, 3, 4, and 6 under 35 U.S.C. 102(b) as being anticipated by Ishizaka, JP-06-111869.

In regards to claims 1, 3, and 6, claims 1, 3, and 6 have been cancelled.

In regards to claim 4, the Examiner's rejection is traversed for the following reason.

Claim 4 of the present invention discloses a connector chip that includes a rectangular parallelepiped insulating substrate having six surfaces and multiple conductive paths formed on an outer peripheral surface. The conductive paths are continuously formed by four of the six surfaces. Insulating layers having a property of repelling molten solder are formed on opposite surfaces between portions of two adjoining conductive paths. Thus, the insulating layers, which repel molten solder, prevent solder from running between the conductive paths and the electrodes when the electrodes are soldered to the chip thereby preventing an electrical short circuit. Therefore, Applicant respectfully contends that Ishizaka does not teach all the features of claim 4. Specifically, Ishizaka does not teach "...insulating layers having

a property of repelling molten solder are formed respectively between portions of two adjoining conductive paths..."

Rather, Ishizaka teaches a terminal 20 that includes an insulator 21 and multiple conductors 22 mounted to the insulator 21 at spaced intervals. The terminal is designed for optimum surface mounting applications whereby the soldering process for the terminal and other parts can be simultaneously performed. Ishizaka, however, does not account for impeding the solder flow between each multiple conductor 22. Specifically, a top surface of the multiple conductors 22 projects above a top surface of the insulator 21. When the terminal 20 is mounted to a circuit board a space exists between each adjacent conductor 22. Thus, during the solder process the flow of solder is not impeded by the insulator because a gap exists between the surface of the insulator 21 and the mounting surface of the circuit board. Because the solder does not contact the insulator there would be no reason to provide an insulator with solder repelling properties. Further, Ishizaka does not disclose or suggest an insulator with solder repelling properties.

Based on the foregoing, it is apparent that Ishizaka does not teach or suggest all the features of claim 4 and therefore cannot be cited as anticipating claim 4. Thus, reconsideration and withdrawal of the rejections of claim 4 based upon Ishizaka are hereby requested.

The Examiner rejected claims 2, 5, and 10 under 35 U.S.C. 103(a) as being unpatentable over Ishizaka, JP-06-111869 in view of Evans, U.S. Pat. No. 3,985,413. The Examiner's rejection is traversed for the following reason.

In regards to claim 2, claim 2 has been cancelled.

In regards to claims 5 and 10, claims 5 and 10 depend from claim 4, thus, all

arguments pertaining to claim 4 are equally applicable to these claims and are herein incorporated by reference.

Further, Applicant submits that Evans does not correct or eliminate the deficiencies of the primary reference, Ishizaka, as they relate to claim 4. Evans discloses an electrical connector for forming connections between conductors on parallel spaced substrates. Evans, however, does not disclose an insulator having solder repelling properties, as required by claim 4 of the present invention. Thus, Evans does not correct or eliminate the deficiencies of Ishizaka as they relate to claim 4. Therefore, Applicant submits that claims 5 and 10 are allowable over the proposed combination of the references.

The Examiner rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Ishizaka, JP-06-111869 in view of Shibata, U.S. Pat. No. 6,123,558. The Examiner's rejection is traversed for the following reason.

Claim 7 depends from claim 4, thus, all arguments pertaining to claim 4 are equally applicable to claim 7 and are herein incorporated by reference.

Further, Applicant submits that Shibata does not correct or eliminate the deficiencies of the primary reference, Ishizaka, as they relate to claim 4. Shibata discloses a card edge connector that includes a slot to receive a circuit card. Shibata, however, does not disclose an insulator having solder repelling properties, as required by claim 4 of the present invention. Thus, Shibata does not correct or eliminate the deficiencies of Ishizaka as they relate to claim 4. Therefore, Applicant submits that claim 7 is allowable over the proposed combination of the references.

The Examiner rejected claims 8 and 9 under 35 U.S.C. 103(a) as being unpatentable over Ishizaka, JP-06-111869. The Examiner's rejection is traversed

for the following reason.

Claims 8 and 9 depend from claim 4, thus, all arguments pertaining to claim 4 are equally applicable to these claims and are herein incorporated by reference.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 18-0160, our Order No. NIS-16657.

Respectfully submitted,

RANKIN, HILL & CLARK LLP

By /Ronald S. Nolan/
Ronald S. Nolan, Reg. No. 59271
Patent Agent

38210 Glenn Avenue
Willoughby, Ohio 44094-7808
(216) 566-9700